

Intel/Altera EP4CE10F17C8N pioneer v2

Overview

This development board is based on EP4CE10F17C8N, BGA256 package.

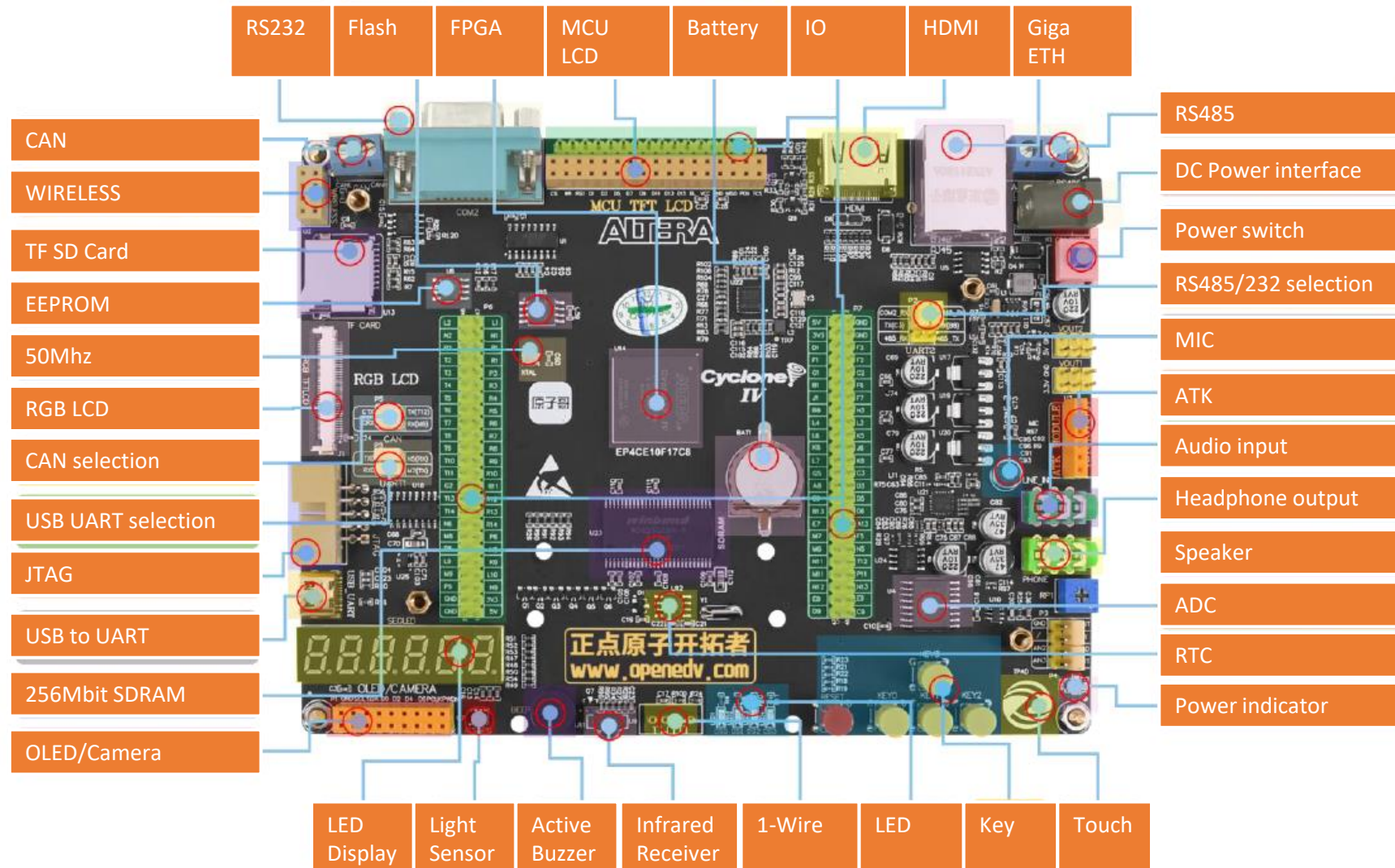
- Abundant interfaces. The board provides a rich set of standard peripheral interfaces, enabling convenient experimentation and development with various peripherals.
- Flexible design. The board adopts a core board plus baseboard structure, with many resources configurable to meet different usage scenarios. Two rows of 24x2 expansion ports are exposed along the edges, providing a total of 88 extended I/O pins.
- Sufficient resources. The board features 1 HDMI port, 1 RGB LCD interface, 1 Gigabit Ethernet port, 1 USB 2.0 SLAVE interface, and various interface chips to meet diverse application requirements.
- User-friendly design. All interfaces are clearly marked with silkscreen labels and outlined with frames for intuitive use. Frequently used peripherals are highlighted with larger silkscreen labels for easy identification. The interface layout is ergonomically designed for convenient access, and resources are rationally allocated to maximize utility.



Order Code

Order Code	Brand	Description
E05001-001	ALIENTEK	Intel/Altera EP4CE10F17C8N pioneer v2

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****Core Specifications:****

- * ****Main Control Chip:**** EP4CE10F17C8N, ****Package:**** BGA256
- * ****Crystal Oscillator:**** 50MHz
- * ****FLASH:**** W25Q16, ****Capacity:**** 16Mbit (2MB)
- * ****SDRAM:**** W9825G6KH-6, ****Capacity:**** 256Mbit (32MB)
- * ****EEPROM:**** AT24C64, ****Capacity:**** 64Kbit (8KB)

****Indicators & Basic Components:****

- * 1 x Power Indicator (Blue)
- * 4 x Status LEDs (DS0~DS3: Red)
- * 1 x IR Receiver, bundled with a compact infrared remote control
- * 1 x High-Performance Audio Codec Chip: ES8388
- * 1 x Reset Button (can serve as a reset signal for FPGA program execution)
- * 4 x Function Buttons
- * 1 x Capacitive Touch Button
- 1 x Power Switch (controls power for the entire development board)

****Sensors & Displays:****

- * 1 x Ambient Light Sensor (Chip: AP3216C)
- * 1 x Standard 2.4/2.8/3.5/4.3/7-inch MCU TFT-LCD Interface (supports resistive/capacitive touchscreens)
- * 1 x Standard RGB TFT-LCD Interface
- * 1 x OLED/Camera Module Interface

****Audio Components:****

- * 1 x Microphone (MIC)
- * 1 x Audio Input Interface
- * 1 x Audio Output Interface
- * 1 x Small Speaker (on the back of the board)

****Communication & Connectivity Interfaces:****

- * 1 x Wireless Module Interface (supports NRF24L01 wireless modules)
- * 1 x CAN Interface (Chip: TJA1050)
- * 1 x 485 Interface (Chip: TP3485)
- * 1 x RS232 Serial Port (Female) Interface (Chip: TP3232)
- * 1 x 1-Wire Interface (supports sensors like DS18B20/DHT11)
- * 1 x ATK Module Interface (supports Alpha & Omega Bluetooth/GPS/MPU6050/RGB LED modules)
- * 1 x USB Serial Port
- * 1 x SD Card Interface (on the front of the board)
- * 1 x Gigabit Ethernet Interface (Chip: YT8531)
- * 1 x HDMI Interface
- * 1 x Standard JTAG Debug/Download Port
- * 1 x RS232/RS485 Select Interface
- * 1 x USB Serial Port Select Interface
- * 1 x CAN Select Interface

****Power & Expansion:****

- * 1 x Set of Multi-function Ports (DAC/ADC/TPAD)
- * 1 x Set of 5V Power Supply/Input Ports
- * 1 x Set of 3.3V Power Supply/Input Ports
- * 1 x DC Power Input Interface (Input Voltage Range: DC 6~16V)
- * 1 x RTC Backup Battery Holder, includes battery (on the back of the board)

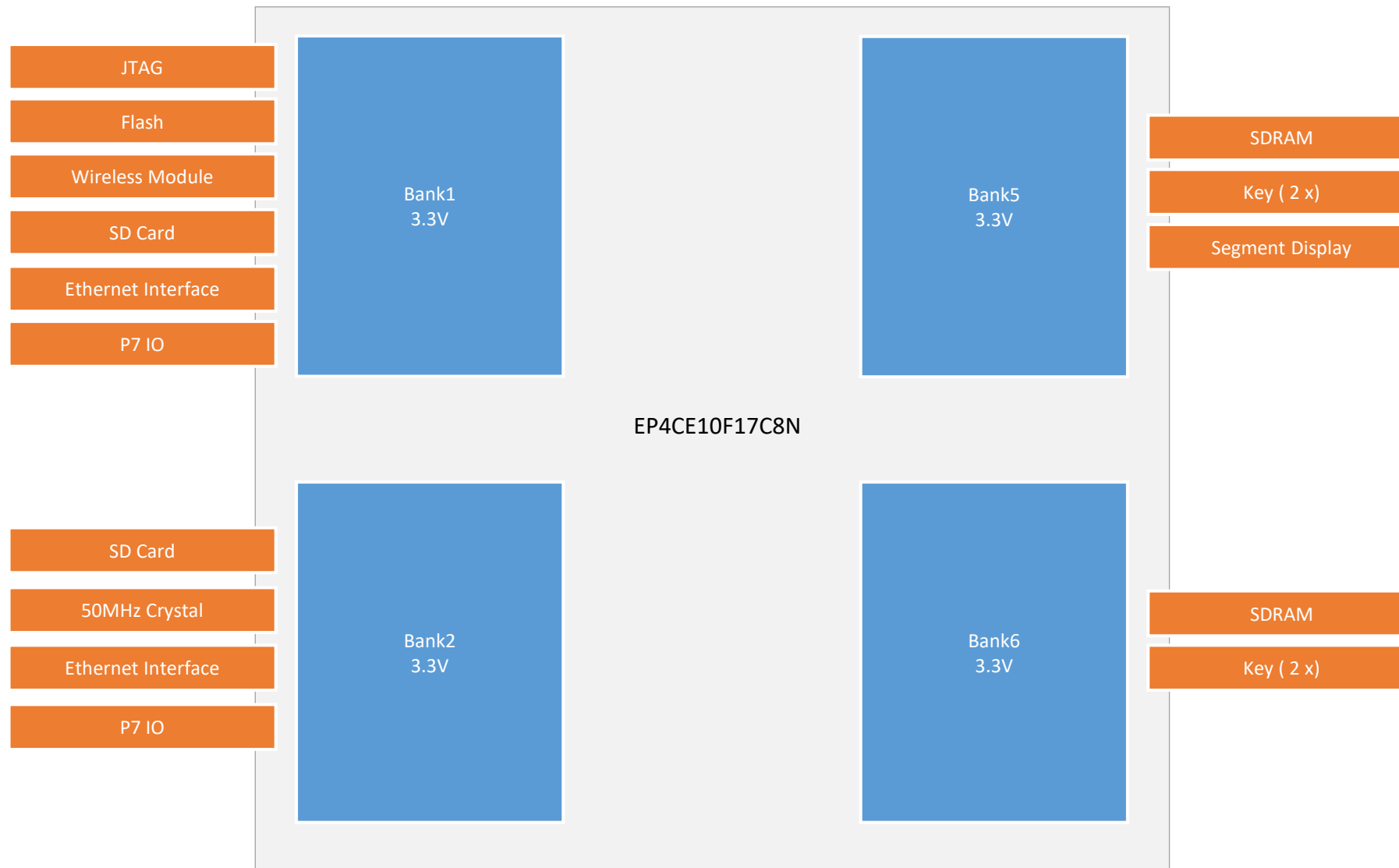
****Additional ICs:****

- * 1 x RTC Real-Time Clock (Chip: PCF8563)
- * 1 x ADC/DAC Conversion Chip (PCF8591)
- 1 x Active Buzzer

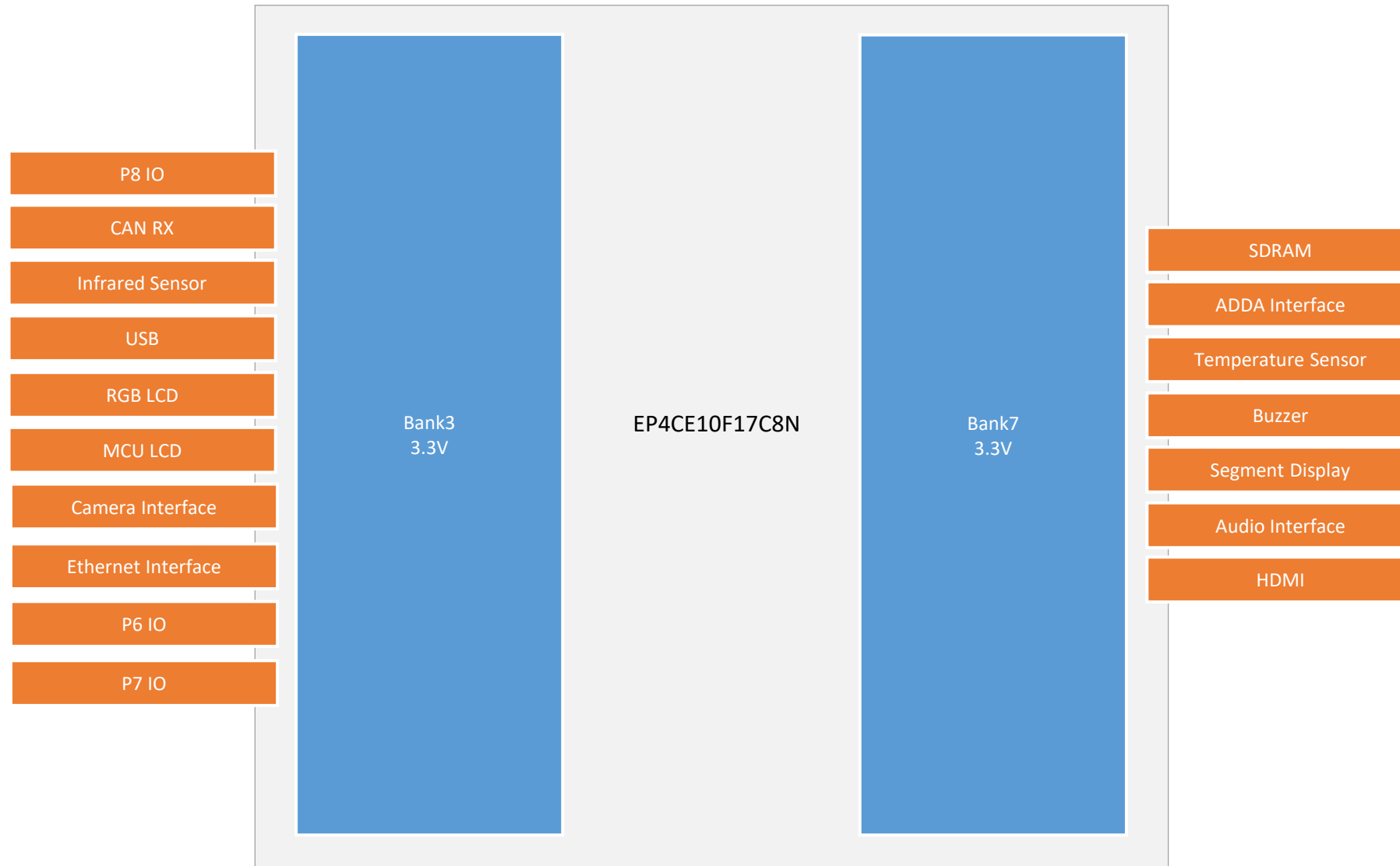
****Expansion:****

- * Two 24x2 expansion ports, providing a total of 88 extended I/O pins (excluding power and ground)

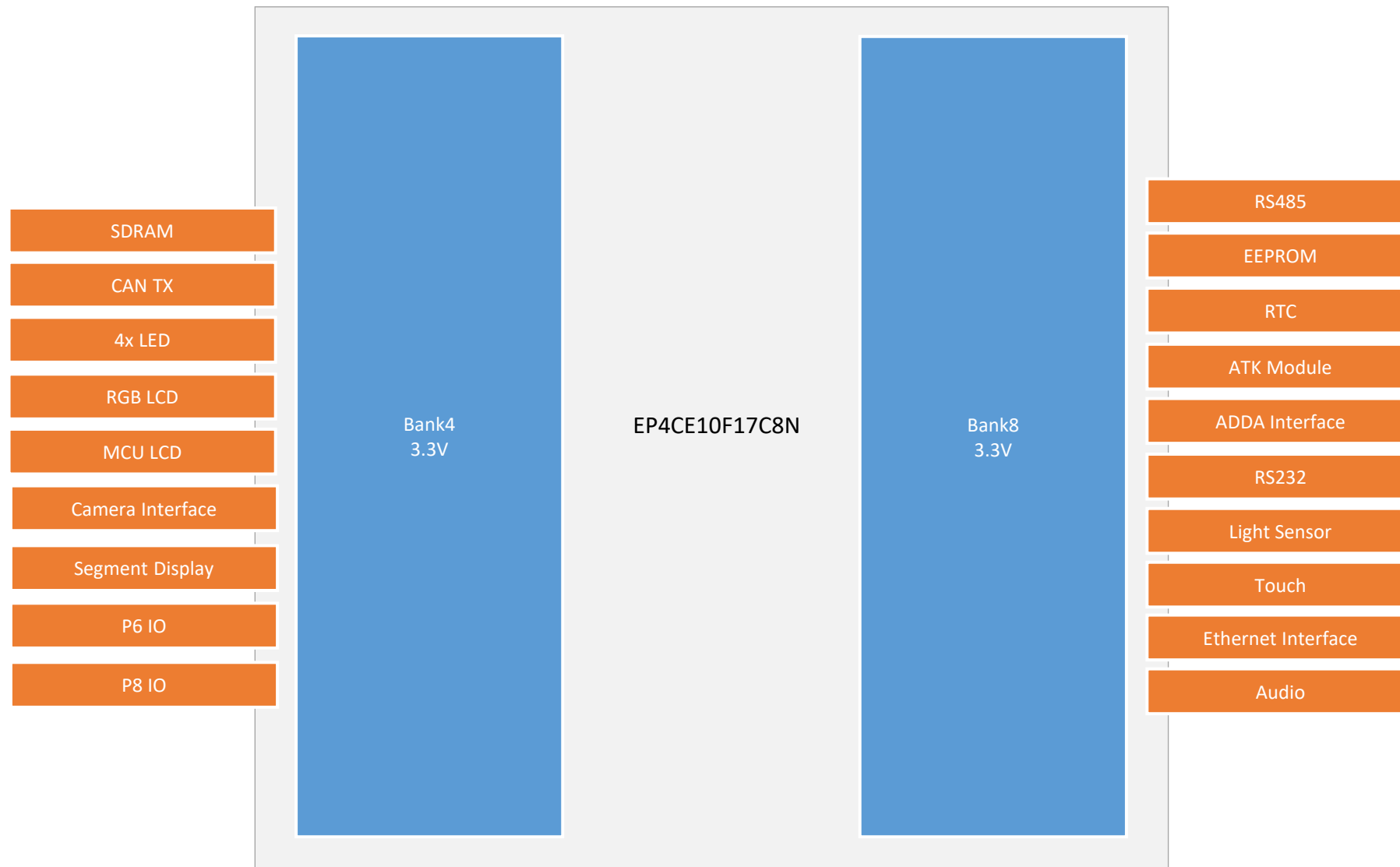
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****1) CAN Interface****

The Pioneer FPGA development board features an onboard CAN bus communication interface. The CAN interface connects to an external CAN bus via two ports: CANH and CANL. Please note: During CAN communication, CANH must be connected to CANH and CANL to CANL. Incorrect connections may result in communication failure!

****2) WIRELESS Module Interface****

The Pioneer FPGA development board includes a wireless module expansion interface. By inserting an NRF24L01 module into this interface, wireless communication can be achieved, enabling wireless functionality for the board. Please note that wireless communication requires two development boards and two wireless modules operating simultaneously. A single board or module alone cannot establish wireless communication.

****3) SD Card Interface****

The Pioneer FPGA development board is equipped with a standard SD card slot (compatible with TF cards), located on the back of the board. SD cards can be inserted and driven using SPI/SDIO protocols, meeting the needs for mass data storage.

****4) Extended I/O Ports (Three Locations in Total)****

The Pioneer FPGA development board features three sets of extended I/O ports: P6, P7, and P8. Among them, P6 and P7 use 2x24 pin headers to provide a total of 88 I/O pins (excluding power and ground). P8 uses a 1x16 pin header, sequentially providing 16 I/O pins from D0 to D15.

****5) RGB TFT-LCD Interface****

The Pioneer FPGA development board includes an RGB LCD interface, which can connect to various Alpha & Omega RGB LCD screen modules and supports touch functionality (both resistive and capacitive screens). To save I/O pins, the RGB565 format is adopted. While this reduces color depth, it conserves I/O resources, and the RGB565 data format is more universally compatible in programming.

****6) 50MHz Crystal Oscillator****

The Pioneer FPGA development board features a 50MHz crystal oscillator (XTAL). The clock signal generated by this oscillator serves as the fundamental clock source for the FPGA. All other required clock frequencies are derived from this base clock using a PLL (Phase-Locked Loop) or other frequency division methods.

****7) CAN Selection Interface****

The Pioneer FPGA development board includes a CAN communication selection interface (P5). When performing CAN communication experiments, jumper caps must be used to connect the pins: CTX to T12 (TX) and CRX to M6 (RX). When jumper caps are not installed, the N3 and M6 pins can also be used as extended I/O ports.

****8) USB Serial Port Selection Interface****

The Pioneer FPGA development board includes a USB serial port selection interface (P9). When conducting USB UART communication experiments, jumper caps must be used to connect the pins: TXD to N5 (RX) and RXD to M7 (TX). When jumper caps are not installed, the N5 and M7 pins can also be used as extended I/O ports.

****9) JTAG Interface****

The Pioneer FPGA development board features a standard 10-pin JTAG debug port. This JTAG port can be directly connected to an FPGA downloader (debugger) for programming or online debugging of the FPGA.

****10) USB to Serial Port****

The Pioneer FPGA development board features an onboard USB serial port (USB_232). This design addresses the declining availability of traditional serial ports on modern computers, especially laptops, which rarely include them. The integrated USB serial port facilitates convenient experimentation with USB UART communication. For flexibility, the corresponding pins are not directly connected on the board. Additionally, this USB port can supply power to the development board. However, its maximum current output is limited to 500mA. When performing experiments with higher power demands, such as LCD display or high-speed AD/DA applications, it is recommended to use the DC 6~16V power input interface.

****11) SDRAM****

The Pioneer FPGA development board is equipped with an SDRAM chip (U23), model W9825G6KH, with a capacity of 256Mbit (32MB). This ample memory easily handles various high-memory-demand scenarios, such as camera image data storage and audio recording data storage.

****12) 6-Digit 7-Segment Display****

The Pioneer FPGA development board includes a 6-digit common anode 7-segment display (SEGLED). This display provides a simple and intuitive way to show information, such as temperature values or light intensity.

****13) Small Speaker****

An 8Ω 2W small speaker (SPEAKER) is mounted on the back of the Pioneer FPGA development board and can be used for audio playback. Driven directly by the ES8388 audio codec, the speaker has a maximum output power of 0.9W.

****14) OLED/Camera Module Interface****

The Pioneer FPGA development board features an OLED/Camera module interface (P1). For OLED modules, align them to the left (leaving the two rightmost holes unoccupied). For camera modules (provided by Alpha & Omega), the connector will be fully populated. This interface enables experiments with various external modules.

****15) Ambient Light Sensor****

The Pioneer FPGA development board includes an ambient light sensor (U7), which can function as both an ambient light sensor and a proximity sensor. This allows the board to detect changes in ambient light and proximity distance, enabling features like automatic backlight adjustment similar to those found in smartphones.

****16) Active Buzzer****

The Pioneer FPGA development board features an active buzzer (BEEP) for generating simple alarm sounds or alerts.

****17) IR Receiver****

The Pioneer FPGA development board includes an IR receiver (U11), enabling infrared remote control functionality. This receiver can detect infrared signals from common remote controls, and users can even implement universal IR decoding. With appropriate applications, this receiver can also be used for data transmission.

****18) RTC Real-Time Clock****

The Pioneer FPGA development board features an onboard RTC real-time clock chip (U12), model PCF8563 from PHILIPS. This industrial-grade multifunctional clock/calendar chip supports alarm functions, timer functions, clock output, and interrupt output, enabling various complex timing services.

****19) 1-Wire Interface****

The Pioneer FPGA development board includes a 1-Wire interface (U9) composed of four gold-plated pin headers. It can connect to 1-Wire sensors such as DS18B20 and DHT11. When not in use, the sensors can be detached and utilized elsewhere, offering great flexibility and convenience.

****20) Four LEDs****

The Pioneer FPGA development board is equipped with four LEDs (DS0–DS3). These LEDs are sufficient for general applications and serve as an excellent aid for debugging by indicating program execution status.

****21) Reset Button****

The Pioneer FPGA development board includes a reset button (RESET), which can serve as a reset signal for FPGA program execution. Note that the default reset signal level is high, and it becomes low when the reset button is pressed.

****22) Four Buttons****

The Pioneer FPGA development board features four mechanical buttons (KEY0–KEY3) directly connected to the FPGA's I/O pins. These buttons can serve as input signals for human-computer interaction. The default state of all four button signals is high, and they become low when pressed.

****23) Battery Interface****

The Pioneer FPGA development board includes a power supply interface (BAT1) for the RTC real-time clock. This ensures the clock continues operating when the FPGA board is powered off, preventing the configured date and time from resetting to default values.

****24) Touch Button****

The Pioneer FPGA development board features a capacitive touch input button (TPAD). It operates based on the principle of capacitor charging and discharging to detect touch inputs.

****25) Power Indicator****

The Pioneer FPGA development board includes a blue LED (PWR) to indicate the power status. The LED lights up when the power is turned on and remains off otherwise. This LED allows users to verify the board's power status.

****26) Multifunction Port****

The Pioneer FPGA development board includes an interface (P3 & P4) composed of eight pin headers. This ingeniously designed port combines P3 and P4 to support multiple functions, including ADC sampling, DAC output, PWM DAC output, capacitive touch key detection, and DAC-ADC self-test. All these functions can be achieved simply by connecting a single jumper cap.

****27) Digital-to-Analog/Analog-to-Digital Conversion****

The Pioneer FPGA development board features a DAC/ADC conversion device (U27), model PCF8591. This chip integrates both ADC and DAC functionalities and communicates with the FPGA via the I²C bus interface.

****28) Headphone Output Interface****

The Pioneer FPGA development board includes an audio output interface (PHONE) for connecting 3.5mm headphones. When the ES8388 plays audio, users can listen through headphones plugged into this interface.

****29) Audio Input Interface****

The Pioneer FPGA development board includes an audio input interface (LINE_IN), which can connect to the headphone output of devices like computers or smartphones.

****30) MIC (Microphone)****

The Pioneer FPGA development board includes a microphone input (MIC), directly connected to the ES8388's recording input channel, enabling recording functionality.

****31) ATK Module Interface****

The Pioneer FPGA development board features a universal module interface (U5) compatible with modules developed by Alpha & Omega, such as GPS, Bluetooth, MPU6050, and full-color RGB LED modules. By plugging in the corresponding module, users can directly proceed with development. In the future, more modules compatible with this interface will be developed to enhance expandability.

****32) 3.3V Power Input/Output****

The Pioneer FPGA development board includes a set of 3.3V power input/output pin headers (2x3, VOUT1). These can supply 3.3V power to external devices or accept 3.3V power input to the board. This provides a convenient 3.3V power source (max current 500mA) for experiments.

****33) 5V Power Input/Output****

The Pioneer FPGA development board includes a set of 5V power input/output pin headers (2x3, VOUT2). These can supply 5V power to external devices or accept 5V power input to the board. When powered via USB, the maximum current is 500mA; when using an external power supply, it can reach up to 1000mA.

****34) Power Switch****

The Pioneer FPGA development board includes a power switch (K1) to control the board's power supply. When the switch is turned off, the entire board is powered down, and the power indicator (PWR) turns off accordingly.

****35) DC 6–16V Power Input****

The Pioneer FPGA development board features an external power input port (DC_IN) with a standard DC power jack. The board uses a DC-DC chip (MP2359) to provide efficient and stable 5V power. Thanks to the DC-DC chip, the board has a wide input voltage range, allowing users to easily find a suitable power supply (as long as the output is within DC 6–16V). For high-power consumption scenarios, such as using 4.3-inch/7-inch screens, Ethernet, or high-speed AD/DA, an external power supply is recommended to ensure sufficient current.

****36) RS485 Interface****

The Pioneer FPGA development board includes an RS485 bus interface (RS485), which connects to external 485 devices via two ports. Please note: For RS485 communication, A must connect to A and B to B; incorrect connections may cause communication failure!

****37) Ethernet Interface (RJ45)****

The Pioneer FPGA development board features a Gigabit Ethernet port (ETHNET) for network cable connection, enabling network communication. This port connects to the PHY chip (YT8531) on the board, supporting communication rates of 10Mbps, 100Mbps, and 1000Mbps.

****38) RS232/485 Selection Interface****

The Pioneer FPGA development board includes an RS232/RS485 selection interface (P2). This interface allows users to connect the FPGA pins to either the RS232 or RS485 module to meet different application requirements.

****39) HDMI Interface****

The Pioneer FPGA development board includes an HDMI interface (output only). It can connect to HDMI-compatible displays, allowing the FPGA to drive the display and show color bars, images, or video.

****40) LCD Interface****

The Pioneer FPGA development board features an MCU TFT-LCD module interface (16-bit parallel data), compatible with the full range of Alpha & Omega LCD modules, including 2.4-inch, 2.8-inch, 3.5-inch, 4.3-inch, and 7-inch MCU TFT-LCD modules, with support for resistive/capacitive touch.

****41) FPGA (EP4CE10)****

This is the core chip (U14) of the development board, model EP4CE10F17C8. This cost-effective chip features 10,320 logic elements, 414Kbits of embedded memory, 23 18×18 embedded multipliers, 2 general-purpose PLLs, 10 global clock networks, 8 user I/O banks, and up to 179 user I/Os.

****42) Flash (W25Q16)****

The Pioneer FPGA development board includes a Flash memory chip (U15). Modern large-scale FPGAs are typically based on SRAM architecture, meaning the program is lost after power-off. Therefore, after the FPGA is powered on, an external chip is required to quickly load the program into the FPGA hardware. This external chip must retain the stored program after power loss, serving as the FPGA's configuration chip. The configuration chip stores the FPGA program to ensure it continues functioning after a power cycle. The Pioneer FPGA development board uses the W25Q16 (fully compatible with the EPCS16 chip) as its configuration chip, with a storage capacity of 16Mbit (2MB).

****44) RS232 Interface (Female)****

The Pioneer FPGA development board features an RS232 interface, connected externally via a standard DB9 female connector. This interface allows communication with computers or other devices equipped with serial ports, enabling serial communication functionality.

****45) EEPROM (AT24C64)****

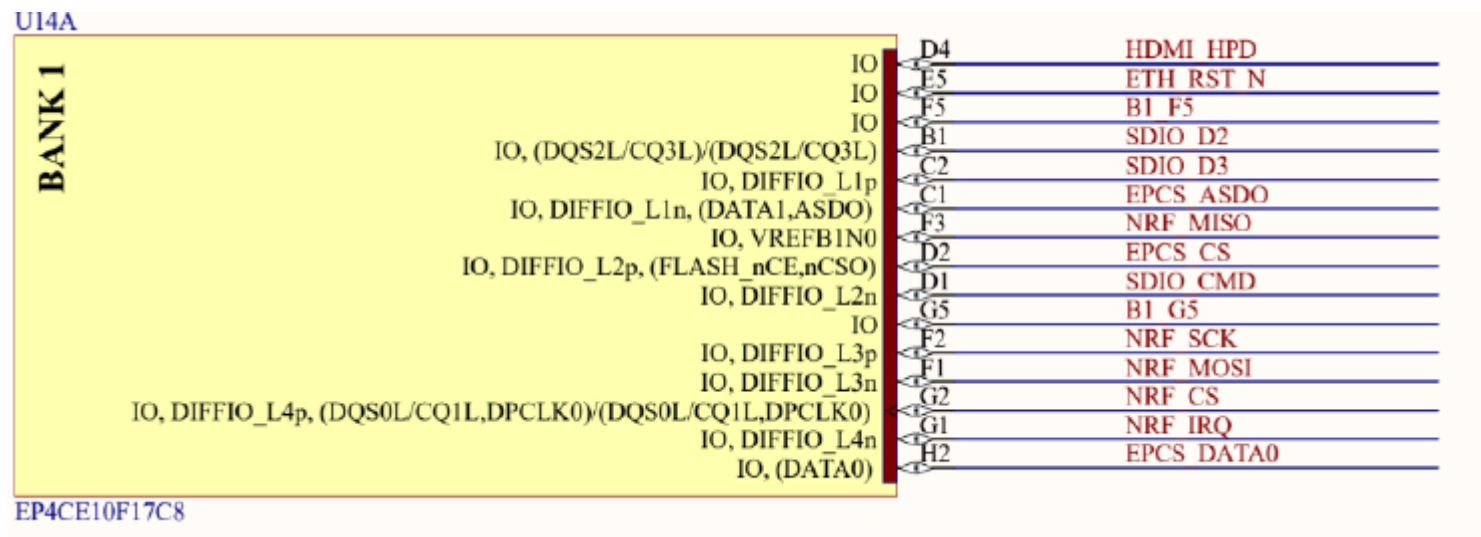
The Pioneer FPGA development board includes an EEPROM chip (U6) with a capacity of 64Kbit (8KB). It is used to store critical data that must not be lost after power-off, such as system configuration parameters. This enables convenient and reliable non-volatile data storage.

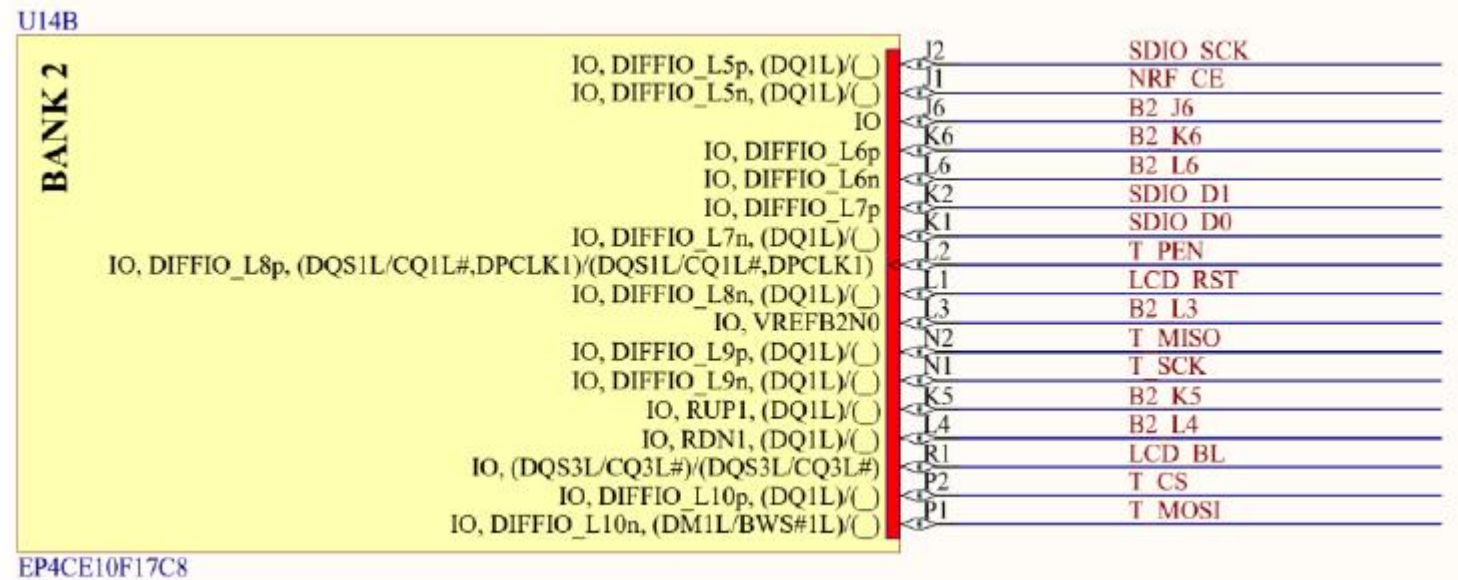
****FPGA Core Chip****

The Pioneer FPGA development board features the Cyclone IV E series EP4CE10F17C8N as its main control chip. This device offers significant advantages in power efficiency and cost-effectiveness. It contains 10,320 logic elements, 414Kbits of embedded memory resources, 23 embedded 18×18 multipliers, 2 general-purpose phase-locked loops (PLLs), 10 global clock networks, 8 user I/O banks, and up to 179 user I/O pins. Understanding the overall hardware resources of the device helps designers optimize their implementations based on available resources to achieve the best performance-to-cost ratio.

****FPGA Bank Schematic****

The onboard FPGA chip of the Pioneer board has a total of 256 I/O pins (with 179 available user I/O). Organizing this large number of I/O pins without structure would be highly impractical. Therefore, the FPGA manufacturer groups these I/O pins into separate blocks, known as I/O banks. The EP4CE10F17C8N contains 8 I/O banks, each of which can be powered by different voltage levels. The schematic diagram of the I/O banks is shown below:

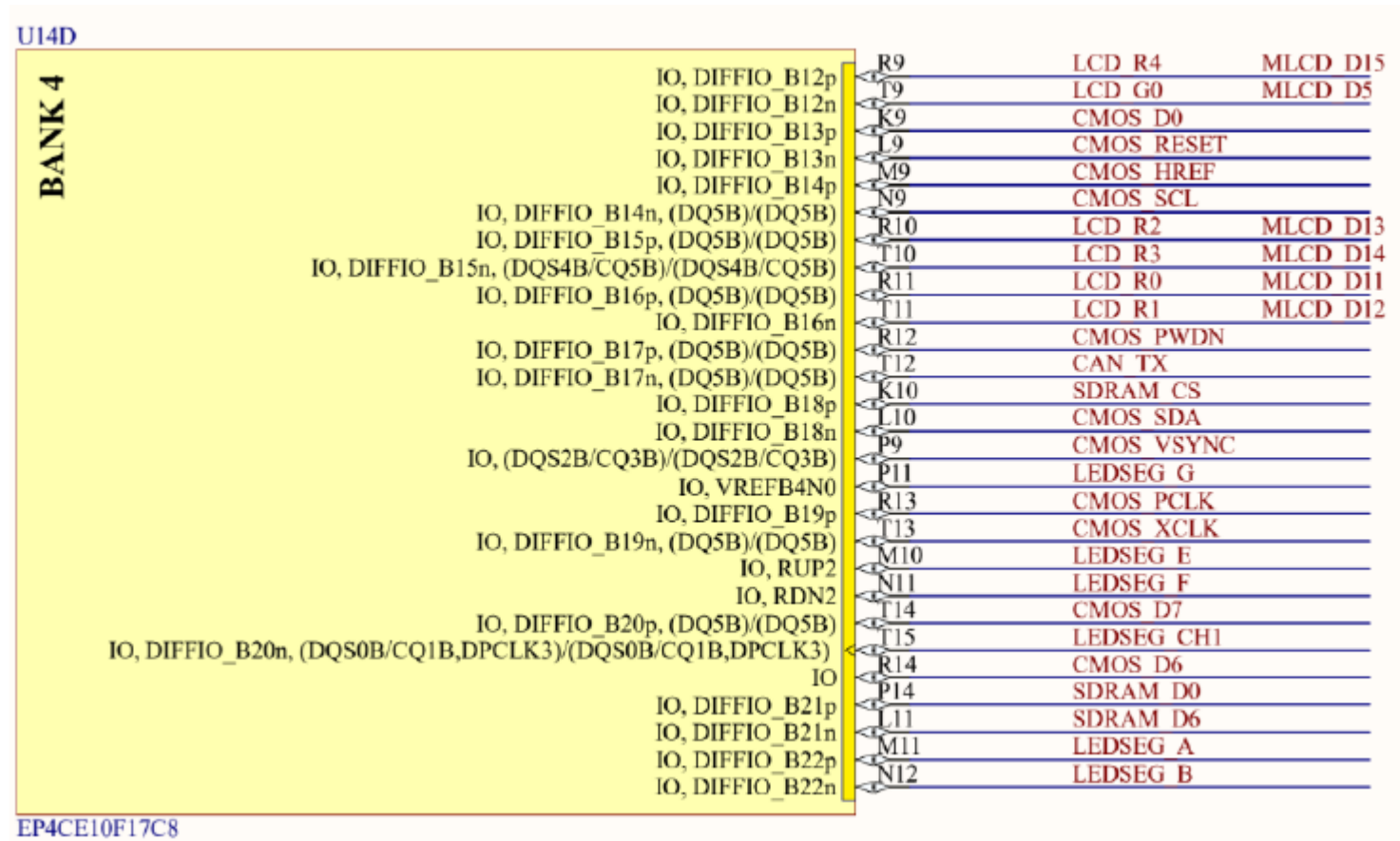


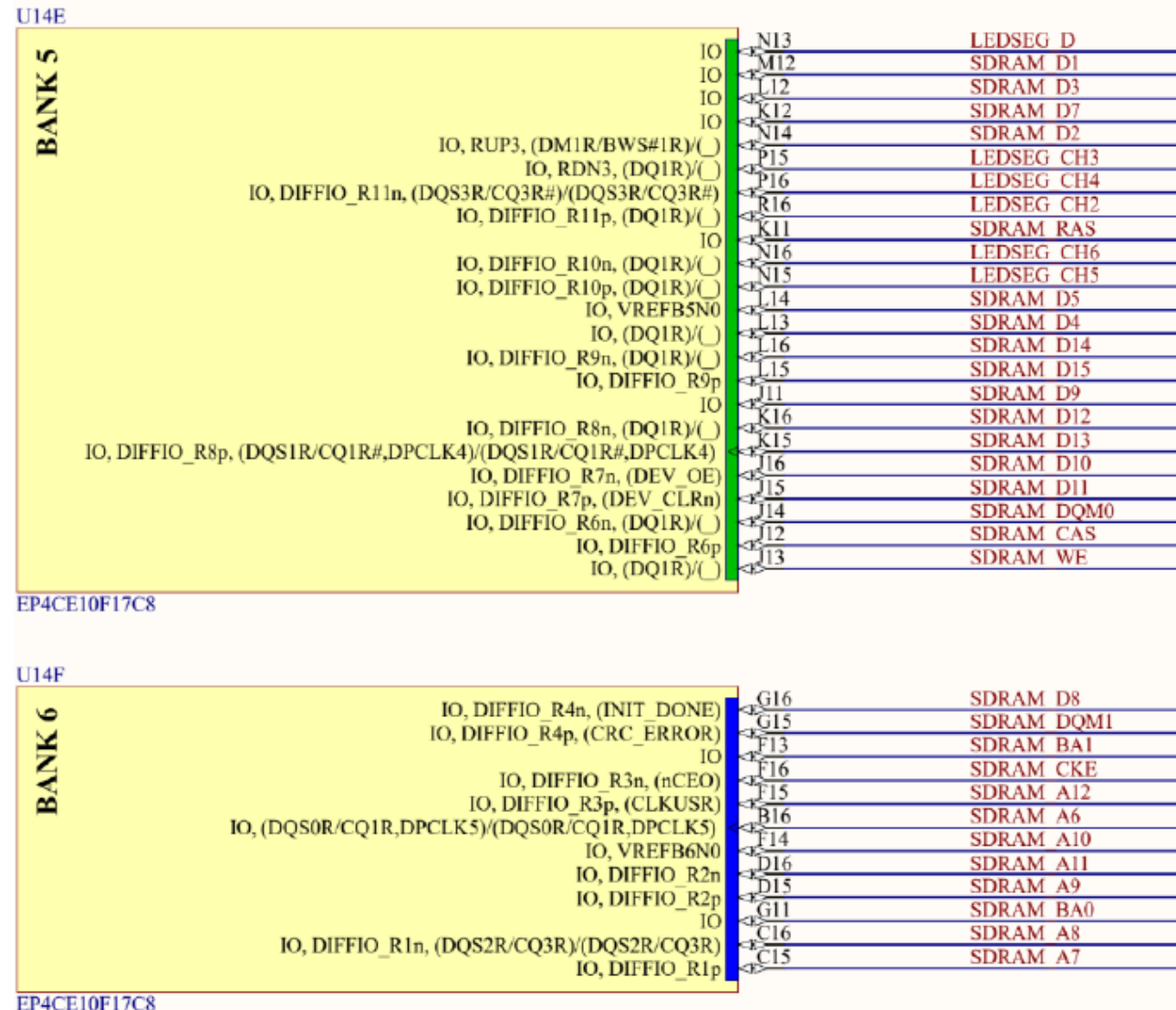


UI4C

BANK 3	IO, DIFFIO_B1p	N3	B3 N3
	IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM5B/BWS#5B)	P3	LCD VSYNC MLCD RS
	IO, DIFFIO_B2p, (DQ3B)/(DQ5B)	R3	LCD CLK MLCD RD
	IO, DIFFIO_B2n	T3	LCD HSYNC MLCD WR
	IO, (DQS1B/CQ1B#,DPCLK2)/(DQS1B/CQ1B#,DPCLK2)	T2	LCD DE MLCD CS
	IO, PLL1_CLKOUTp	R4	LCD B3 MLCD D3
	IO, PLL1_CLKOUTn	T4	LCD B4 MLCD D4
	IO, DIFFIO_B4p, (DQ3B)/(DQ5B)	N5	UART1 RX
	IO, DIFFIO_B4n, (DQ3B)/(DQ5B)	N6	CMOS D5
	IO, (DQ3B)/(DQ5B)	M6	CAN RX
	IO, VREFB3N0	P6	CMOS D4
	IO, DIFFIO_B5p, (DQS3B/CQ3B#)/(DQS3B/CQ3B#)	M7	UART1 TX
	IO, DIFFIO_B5n	K8	B3 K8
	IO, DIFFIO_B6p, (DQ3B)/(DQ5B)	R5	LCD B1 MLCD D1
	IO, DIFFIO_B6n	T5	LCD B2 MLCD D2
	IO, DIFFIO_B7p, (DQ3B)/(DQ5B)	R6	LCD G5 MLCD D10
	IO, DIFFIO_B7n	T6	LCD B0 MLCD D0
	IO, (DQ3B)/(DQ5B)	L7	B3 L7
	IO, DIFFIO_B8p, (DQ3B)/(DQ5B)	R7	LCD G3 MLCD D8
	IO, DIFFIO_B8n, (DQS5B/CQ5B#)/(DQS5B/CQ5B#)	T7	LCD G4 MLCD D9
	IO, DIFFIO_B9p, (DQ3B)/(DQ5B)	L8	REMOTE IN
	IO, DIFFIO_B9n, (DM5B/BWS#5B)/(DM5B/BWS#5B)	M8	CMOS D3
	IO, DIFFIO_B10p, (DQ5B)/(DQ5B)	N8	CMOS D2
	IO, DIFFIO_B10n, (DQ5B)/(DQ5B)	P8	CMOS D1
	IO, DIFFIO_B11p	R8	LCD G1 MLCD D6
	IO, DIFFIO_B11n	T8	LCD G2 MLCD D7

EP4CE10F17C8





U14G

BANK 7

IO, DIFFIO_T21n	C14	SDRAM A3
IO, DIFFIO_T21p, (DQ5T)/(DQ5T)	D14	SDRAM A2
IO, DIFFIO_T20n	D11	LED0
IO, DIFFIO_T20p, (DQS0T/CQ1T, DPCLK6)/(DQS0T/CQ1T, DPCLK6)	D12	BEEP
IO, DIFFIO_T19n	A13	I2S LRCK
IO, DIFFIO_T19p, (DQ5T)/(DQ5T)	B13	I2S SCLK
IO, PLL2_CLKOUTn	A14	SDRAM A4
IO, PLL2_CLKOUTp	B14	SDRAM CLK
IO, RUP4	E11	SDRAM A1
IO, RDN4	E10	LED2
IO, DIFFIO_T18n, (DQ5T)/(DQ5T)	A12	HDMI FCLK N
IO, DIFFIO_T18p, (DQ5T)/(DQ5T)	B12	HDMI FCLK P
IO, DIFFIO_T17n, (DQ5T)/(DQ5T)	A11	HDMI FD0 N
IO, DIFFIO_T17p, (DQ5T)/(DQ5T)	B11	HDMI FD0 P
IO, VREFB7N0	C11	LED1
IO, DIFFIO_T16n	F10	1WIRE DQ
IO, DIFFIO_T16p, (DQS2T/CQ3T)/(DQS2T/CQ3T)	F9	LED3
IO, DIFFIO_T15n	F11	SDRAM A0
IO, DIFFIO_T15p	A15	SDRAM A5
IO, DIFFIO_T14n, (DQ5T)/(DQ5T)	A10	HDMI FD1 N
IO, DIFFIO_T14p, (DQ5T)/(DQ5T)	B10	HDMI FD1 P
IO, DIFFIO_T13n, (DQ5T)/(DQ5T)	C9	LEDSEG C
IO, DIFFIO_T13p, (DM5T/BWS#5T)/(DM5T/BWS#5T)	D9	LEDSEG DOT
IO, (DQS4T/CQ5T)/(DQS4T/CQ5T)	E9	ADDA SCL
IO, DIFFIO_T12n	A9	HDMI FD2 N
IO, DIFFIO_T12p	B9	HDMI FD2 P

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U14H

BANK 8	IO, DIFFIO_T11n	A8	UART3 TX
	IO, DIFFIO_T11p	B8	UART2 RX
	IO, (DQS5T/CQ5T#)/(DQS5T/CQ5T#)	C8	IIC SDA
	IO, (DQ3T)/(DQ5T)	D8	IIC SCL
	IO, DIFFIO_T10n, (DATA2), (DQ3T)/(DQ5T)	E8	ADDA SDA
	IO, DIFFIO_T10p, (DATA3)	F8	TPAD
	IO, DIFFIO_T9n, (DQ3T)/(DQ5T)	A7	ETH TXD3
	IO, DIFFIO_T9p, (DATA4), (DQ3T)/(DQ5T)	B7	ETH TXD2
	IO, DIFFIO_T8n	F6	ETH MDIO
	IO, DIFFIO_T8p	F7	ETH MDC
	IO, VREFB8N0	C6	I2S ADCDAT
	IO, DIFFIO_T7n, (DQS3T/CQ3T#)/(DQS3T/CQ3T#)	A6	ETH TXD1
	IO, DIFFIO_T7p, (DQ3T)/(DQ5T)	B6	ETH TXD0
	IO, (DATA5), (DQ3T)/(DQ5T)	E7	I2S MCLK
	IO, (DATA6), (DQ3T)/(DQ5T)	E6	UART3 RX
	IO, DIFFIO_T6n, (DATA7), (DQ3T)/(DQ5T)	A5	ETH TXC
	IO, DIFFIO_T5n	A2	ETH RXD3
	IO, DIFFIO_T5p, (DQ3T)/(DQ5T)	B5	ETH TX EN
	IO, DIFFIO_T4n, (DM3T/BWS#3T)/(DM5T/BWS#5T)	A4	ETH RX DV
	IO, DIFFIO_T4p	B4	ETH RXD0
	IO, DIFFIO_T3n	D5	GBC KEY
	IO, DIFFIO_T3p	D6	I2S DACDAT
	IO, DIFFIO_T2n	A3	ETH RXD1
	IO, DIFFIO_T2p, (DQS1T/CQ1T#,DPCLK7)/(DQS1T/CQ1T#,DPCLK7)	B3	ETH RXD2
	IO, DIFFIO_T1n	C3	UART2 TX
	IO, DIFFIO_T1p	D3	GBC LED

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Revision History

Date	Revision	Change description
30/10/2025	1.0	Initial release