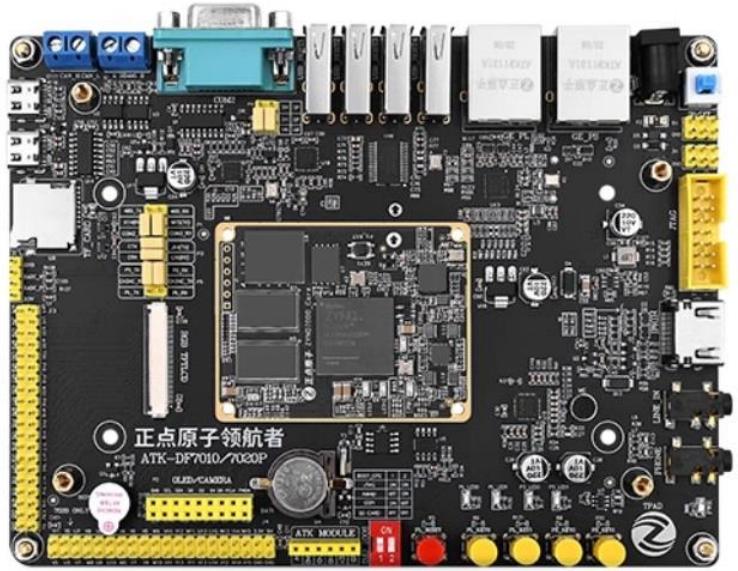
AMD/Xilinx ZYNQ XC7Z010 pilot v2

Overview

This development board is based on XC7Z7010, CLG400 package.

- Abundant Interfaces. The development board offers a wide range of standard peripheral interfaces, enabling convenient experimentation and development with various peripherals.
- Flexible Design. Adopting a core board + carrier board structure, many resources on the development board can be flexibly configured to meet different usage conditions. Two rows of 20×2 expansion headers (J4 expansion port is only available for the ZYNQ 7020 core board) are exposed along the board edge, providing a total of 72 extended I/O pins.
- Sufficient Resources. The board is equipped with a high-performance audio codec chip, an HDMI interface, an RGB LCD interface, one PL Gigabit Ethernet port, one PS Gigabit Ethernet port, four USB HOST interfaces, one USB SLAVE interface, and various interface chips, meeting the requirements of diverse applications.
- User-Friendly Design. All interfaces are clearly marked with silkscreen labels and outlined with boxes for intuitive use. Frequently used peripherals are highlighted with large silkscreen labels for easy identification. The interface layout is thoughtfully designed for ergonomic accessibility, and resources are reasonably allocated to maximize utility.



Order Code

Order Code	Brand	Description
E05004-001	ALIENTEK	AMD/Xilinx ZYNQ XC7Z010 pilot v2

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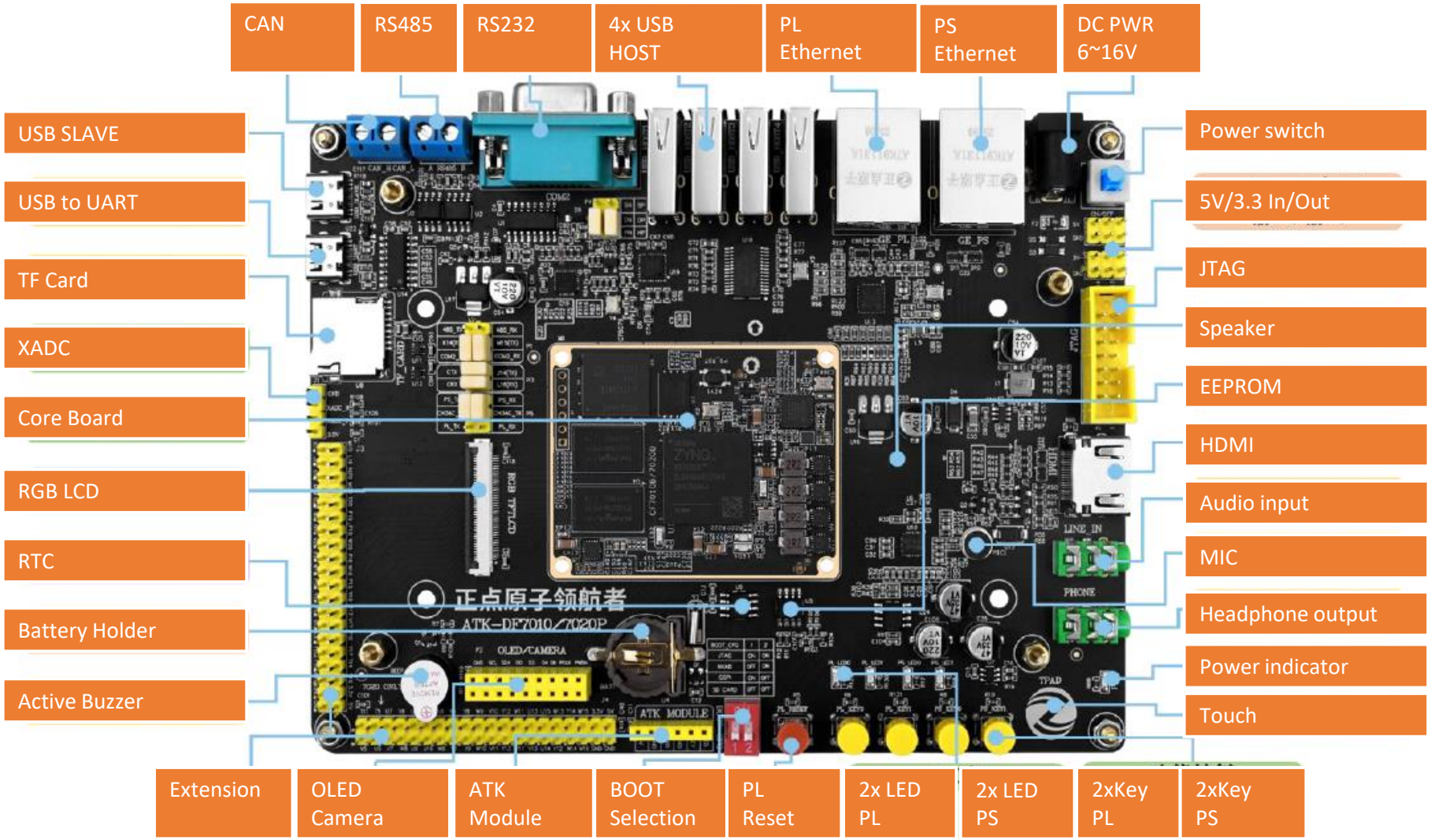

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- 1 Core Board Connector Interface (one on top and one on bottom), compatible with ZYNQ 7020/ZYNQ 7010 core boards.
- EEPROM Chip: AT24C64, 64 Kbit (8 KB) capacity.
- 1 Power Indicator (Blue)
- 2 PL LEDs (Red)
- 2 PS LEDs (Red)
- 1 Active Buzzer
- 1 PL Reset Button
- 2 PL Function Buttons
- 2 PS Function Buttons
- 1 Capacitive Touch Button
- 1 CAN Bus Interface, using TJA1050 transceiver chip.
- 1 RS232 Serial Port Interface (DB9 Female Connector)
- 1 RS485 Interface (shares I/O with the RS232 interface)
- 1 RS232/RS485 Selection Jumper
- 1 CAN Bus Selection Jumper
- 1 Standard RGB888 TFT-LCD Interface
- 1 XADC Interface
- 1 OLED/Camera Module Interface
- Two 20x2 Expansion Headers, providing a total of 72 extended I/O pins (J4 header is only available for the ZYNQ-7020 core board). Each includes one 3.3V and one 5V power pin.
- 1 RTC (Real-Time Clock), chip model PCF8563.
- 1 RTC Battery Holder with CR1220 battery included.
- 1 ATK MODULE Interface, compatible with Alpha Bluetooth / GPS / UART modules.
- 1 BOOT Mode Selection Switch
- 1 Audio Output Interface
- 1 Audio Input Interface
- 1 High-Performance Audio Codec Chip (ES8388), supports recording, line-in, and audio playback.
- 1 Microphone (MIC)
- 1 Small Speaker (located on the back of the board)

- 1 HDMI Output Interface
- 4 USB HOST Interfaces
- 1 USB SLAVE Interface
- 14-Pin JTAG Interface for board programming and debugging.
- 1 set of 5V Power Supply/Input Terminals
- 1 set of 3.3V Power Supply/Input Terminals
- 1 Power Switch for the entire development board.
- 1 DC Power Input Jack (Input Voltage Range: DC 6V ~ 16V)
- 1 PL Gigabit Ethernet Interface (RJ45)
- 1 PS Gigabit Ethernet Interface (RJ45)
- 1 Micro SD (TF_CARD) Card Interface
- 1 USB-to-Serial Port

Baseboard Peripherals & Interfaces:

1. **Active Buzzer:** One on-board active buzzer (BEEP) for simple alarms or alerts.
2. **PL Reset Button:** One PL reset button (PL_RESET) providing a reset signal for the ZYNQ's Programmable Logic. The signal is normally high and goes low when pressed.
3. **PL LEDs:** Two red PL LEDs (PL_LED0~PL_LED1) connected directly to PL I/O pins, useful for indicating program status during debugging.
4. **PL Function Buttons:** Two mechanical buttons (PL_KEY0~PL_KEY1) connected directly to PL I/O pins, serving as user input. They are normally high and go low when pressed.
5. **PS LEDs:** Two red PS LEDs (PS_LED0~PS_LED1) connected directly to PS I/O pins.
6. **PS Function Buttons:** Two mechanical buttons (PS_KEY0, PS_KEY1) connected directly to PS I/O pins, serving as user input. They are normally high and go low when pressed.
7. **Touch Button:** One capacitive touch button (TPAD), implemented using the JL223B (compatible with AR101) chip, which detects touch via capacitance charging/discharging. Outputs high when touched, low when released.
8. **USB to UART:** One PS-side USB-to-UART bridge for serial communication experiments. *Note: This USB port can also power the board, but is limited to 500mA, which may be insufficient for the ARM processor; using a dedicated power adapter is recommended.*
9. **RS232 Interface (DB9 Female):** One RS232 interface via a standard DB9 female connector for connecting to PCs or other serial devices.
10. **RS485 Interface:** One RS485 interface via a 2-pin terminal block for connecting to other RS485 devices. *Important: For communication, A must connect to A and B to B.*
11. **RGB TFT-LCD Interface:** One RGB LCD interface supporting various ALIENTEK RGB LCD screens using RGB888 format (16.77 million colors), often with touch support.
12. **XADC Interface:** One XADC interface whose signals connect directly to the ZYNQ's XADC pins, for measuring external analog voltages (0~1V range). The internal XADC can also monitor the ZYNQ chip's temperature and voltage.
13. **OLED/Camera Module Interface:** One interface for ALIENTEK OLED displays or camera modules, allowing direct connection for respective experiments.
14. **EEPROM (AT24C64):** One I2C EEPROM chip, 64Kbit (8KB) capacity, for storing non-volatile data like system parameters.
15. **RTC (Real-Time Clock):** One RTC chip (PCF8563), an industrial-grade clock/calendar chip with alarm, timer, and interrupt functions.
16. **Battery Interface:** One RTC backup power interface to maintain the clock when the main board power is off.
17. **ATK MODULE Interface:** One ALIENTEK universal module interface, supporting various modules like GPS, Bluetooth, MPU6050, RGB LED, OLED, etc., for easy expansion.

Baseboard Peripherals & Interfaces:

18. **BOOT Mode Selection Switch:** One switch (BOOT_CFG) to set the PS boot source (e.g., JTAG, QSPI FLASH, SD Card).
19. **Power Indicator:** One blue LED (PWR) indicating the board's power status (on when powered).
20. **Headphone Output (PHONE):** One 3.5mm audio output jack for headphones, driven by the ES8388 codec.
21. **Audio Line Input (LINE_IN):** One audio input jack for connecting to line-level outputs from devices like PCs or phones.
22. **Microphone (MIC):** One onboard microphone input connected to the ES8388 for recording functionality.
23. **Speaker:** One small onboard speaker (SPEAKER) driven directly by the ES8388 for audio playback.
24. **HDMI Interface:** One HDMI output interface. *Note: As there is no dedicated HDMI PHY chip, the HDMI encoding is implemented using the ZYNQ PL logic.*
25. **14-Pin JTAG Interface:** One standard 14-pin JTAG debug port, functionally connected to the core board's 6-pin JTAG, for programming and debugging with an FPGA downloader/debugger.
26. **3.3V Power Input/Output:** One set of 2x3 pin headers for providing 3.3V power to external components or accepting 3.3V input to power the board (Max current: 1000mA).
27. **5V Power Input/Output:** One set of 2x3 pin headers for providing 5V power to external components or accepting 5V input to power the board (Max current: 500mA via USB, 1000mA via power adapter).
28. **Power Switch:** One main power switch controlling all power to the development board.
29. **DC 6~16V Power Input (DC_IN):** One standard DC power jack. The wide input range (DC 6V~16V) allows flexibility in choosing a suitable power supply. Using the provided power adapter is recommended for high-power scenarios.
30. **PL Gigabit Ethernet Interface (RJ45):** One PL-side Gigabit Ethernet port (PL_GE) using the YT8531 chip, supporting 10M/100M/1000Mbps rates.
31. **PS Gigabit Ethernet Interface (RJ45):** One PS-side Gigabit Ethernet port (PS_GE) connected via the board-to-board connector to the core board's PHY, supporting 10M/100M/1000Mbps rates.
32. **USB 2.0 Interfaces:** Includes four USB HOST ports for connecting devices like mice/keyboards, and one USB SLAVE port for connecting to a host computer. A dedicated USB PHY chip is used for the PS USB module.
33. **Micro SD Card Interface (TF_CARD):** One standard Micro SD card slot, supporting SPI/SDIO modes for mass storage.
34. **CAN Interface:** One CAN bus interface via a 2-pin terminal block. *Important: For communication, CANH must connect to CANH and CANL to CANL.*
35. **40-Pin Expansion Headers:** Two 2x20 pin 40-pin expansion headers (J4 is for ZYNQ7020 core board only), located on the board edge. They provide 72 I/O pins, 2x +3.3V, 2x +5V, and 4x GND, for connecting modules like high-speed AD/DA or dual-camera modules.

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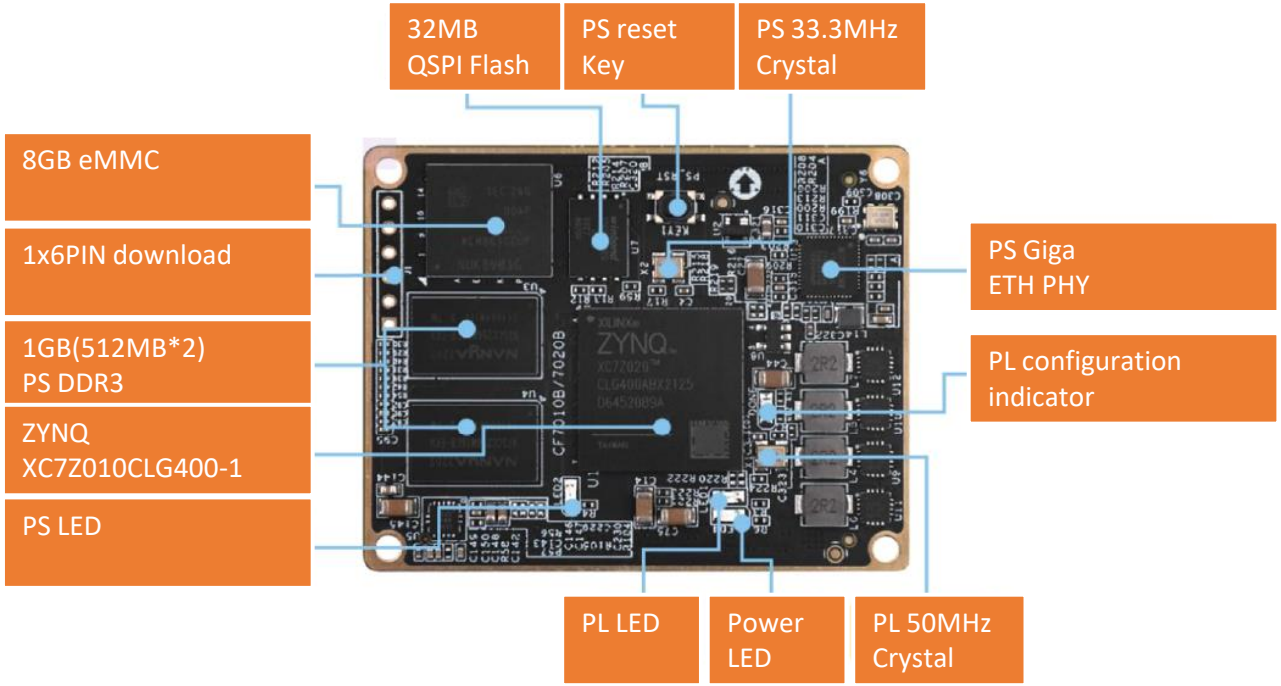

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ZYNQ Chip: Utilizes the Xilinx ZYNQ-7000 series. The chip on the ZYNQ 7020 core board is model XC7Z020CLG400-2, featuring up to 85K Programmable Logic (PL) cells and 4.9 Mbit of Block RAM (BRAM). The chip on the ZYNQ 7010 core board is model XC7Z010CLG400-1, featuring up to 28K PL cells and 2.1 Mbit of BRAM. The Processing System (PS) for both ZYNQ variants is based on a dual-core Cortex-A9 architecture.

Note on Speed Grade: It is important to note that the ZYNQ 7020 core board uses a speed grade of "-2", while the ZYNQ 7010 uses "-1". Consequently, the ZYNQ 7020 core board offers a higher speed grade, supporting higher operating frequencies.

2x DDR3 SDRAM: The ZYNQ 7020 core board uses DDR3 models NT5CC256M16, with each chip providing 4 Gbit, resulting in a total capacity of 8 Gbit (1 GB). The ZYNQ 7010 core board uses DDR3 models NT5CC128M16, with each chip providing 2 Gbit, for a total capacity of 4 Gbit (512 MB).

- 1x 1x6 Download Interface, functionally equivalent to the 14-pin JTAG interface on the baseboard.
- 1x PL LED
- 1x PS LED
- 1x PL Crystal Oscillator: 50MHz, providing the clock for the Programmable Logic.
- 1x PS Crystal Oscillator: 33.333MHz, providing the clock for the Processing System (CPU).
- 1x Power Indicator (Blue)
- 1x PL Configuration Status Indicator (DONE LED, Green)
- 1x PS Gigabit Ethernet PHY Chip: YT8521S
- 1x PS Reset Button
- 1x QSPI FLASH, model W25Q256, 32MB capacity.
- 1x eMMC, model KLM8G1GETF, 8GB capacity.

Core Board Key Components Overview:

1. **ZYNQ Main Controller Chip:**
   * **ZYNQ-7020** core board uses the **XC7Z020CLG400-2**, featuring **85K Logic Cells** and **4.9 Mbit of BRAM**.
   * **ZYNQ-7010** core board uses the **XC7Z010CLG400-1**, featuring **28K Logic Cells** and **2.1 Mbit of BRAM**.
   * The ZYNQ Processing System (PS) integrates a dual-core **Cortex-A9** Application Processing Unit (APU), along with extensive peripheral interfaces, cache memory, memory interfaces, interconnect, and clock generation circuits.

2. **DDR3 SDRAM:**
   * **ZYNQ-7020:** Two onboard **NT5CC256M16** chips, each 4Gbit, totaling **8Gbit (1GB)**.
   * **ZYNQ-7010:** Two onboard **NT5CC128M16** chips, each 2Gbit, totaling **4Gbit (512MB)**.
   * This DDR3 memory easily handles high-memory, high-bandwidth scenarios (e.g., camera image buffer) and serves as the main system memory for the PS.

3. **6-PIN Download Interface:**
   * Integrated with the baseboard's 14-PIN JTAG interface. Allows debugging and programming when using the core board independently.

4. **PL LED:**
   * One red LED connected directly to a PL I/O pin. User-controllable via Verilog code.

5. **PS LED:**
   * One red LED connected directly to a PS I/O pin. User-controllable via C code.

6. **PL 50MHz Crystal Oscillator:**
   * Provides the fundamental clock signal for the Programmable Logic via a dedicated PL clock pin. All other PL clock frequencies are derived from this source.

7. **PS 33.333MHz Crystal Oscillator:**
   * Provides the fundamental clock signal for the Processing System via a dedicated PS clock pin. All other PS clock frequencies are derived from this source.

Core Board Key Components Overview:

8. **Power Indicator:**
   * One blue LED indicating the core board's power status (on when powered).

9. **PL Configuration Status Indicator (DONE LED):**
   * One green LED connected to the PL's DONE pin. Illuminates after the PL configuration (program download) is complete.

10. **PS Gigabit Ethernet PHY Chip:**
   * Onboard **YT8521** PHY chip, implementing the 10M/100M/1000Mbps Ethernet physical layer for the PS. Its transceiver connects to the RJ45 jack on the baseboard.

11. **PS Reset Button:**
   * One button (PS_RST) connected to the PS reset logic. Pressing it resets the PS to its post-power-up state.

12. **QSPI Flash:**
   * One Flash chip, **256Mbit (32MB)** capacity. Used to store the ZYNQ device image, including the PS application and the PL configuration bitstream.

13. **eMMC:**
   * One eMMC chip (non-volatile NAND storage), **8GB** capacity. Serves as a large-capacity "hard drive" for the PS.

Revision History

Date	Revision	Change description
30/10/2025	1.0	Initial release